N CHANNEL ENHANCEMENT MODE POWER MOSFET

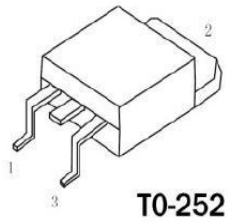
Lead Free Package and Finish

Description:

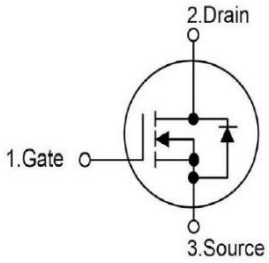
RS60N35D Series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance . it provides the designer with an extreme efficient device for use in a wide range of power applications

The TO-252 package is widely preferred for all commercial industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance

I_D	$R_{DS(ON)}$(Max)	V_{DSS}
35A	20mΩ	60V



Not to Scale



Not to Scale

Features:

- •Lower On-resistance
- •Simple Drive Requirement
- •Fast Switching Characteristic
- •RoHS Compliant

Ordering Information:

Part Number	Package	Marking
RS60N35D	TO-252	RS60N35D

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	A
ID @Tc=25℃	Drain Current	35	
ID @Tc=100℃	Drain Current,Vgs@10V	24	
I_{DM}	Pulsed Drain Current (Note*1)	140	
PD @Tc=25℃	Total Power Dissipation	43	W
Eas	Single pulse avalanche energy (Note*4)	260	mJ
TL TPKG	Maximum Temperature for Soldering Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	300 260	℃
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 175	

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	Value	Units
Rthj-C	Maximum Thermal Resistance,Junction-case	2.9	℃/W
Rthj-a	Maximum Thermal Resistance,Junction-ambient[3]	62.5	℃/W

Electrical Characteristics @TJ=25℃(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain-source Breakdown Voltage	60	--	--	V	VGS=0V,ID=250uA
IDSS	Drain-Source Leakage Current	--	--	10	μA	VDS=60V,VGS=0V
IGSS	Gate-Source Forward Leakage	--	--	100	nA	VGS=+20V VDS=0V
	Gate-Source Reverse Leakage	--	--	-100		VGS=-20V VDS=0V
g_{fs}	Forward Transconductance	--	18	--	S	ID=15A VDS=10V

ON Characteristics (Note*3) TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain-Source On-Resistance	--	16	20	mΩ	VGS=10V,ID=20A
VGS(TH)	Gate Threshold Voltage	1.4	1.7	2.5	V	VGS=VDS,ID=250μA

Resistive Switching Characteristics (Note*4) Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(on)	Turn-on Delay Time	--	7.2	--	nS	VDS=30V ID=20A Rg=3.3Ω Vgs=10V
trise	Rise Time	--	10.8	--		
td(off)	Turn-OFF Delay Time	--	22	--		
tfall	Fall Time	--	4.7	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1964	--	pF	VGS=0V VDS=30V f=1.0MHz
Coss	Output Capacitance	--	100	--		
Crss	Reverse Transfer Capacitance	--	85	--		
Qg	Total Gate Charge	--	32	--	nC	VDS=48V ID=20A VGS=10V
Qgs	Gate-Source Charge	--	4.2	--		
Qgd	Gate-Drain("Miller"）Charge	--	12	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
VSD	Diode Forward Voltage (Note*3)	--	--	1.2	V	IS=15A,VGS=0V
ISD	Diode Forward Current (Note*2)			35	A	
trr	Reverse Recovery Time	--	27	--	nS	VGS=0V IS=15A,di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	38	--	nC	

Notes:

*1.Pulse width limited by max.junction temperature
*2.Surface Mounted on FR4 Board, t ≤ 10 sec.
*3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
*4. EAS condition : Tj=25 ,VDD= ℃ 30V,VG=10V,L=0.5mH,Rg=25Ω

Typical Feature curve

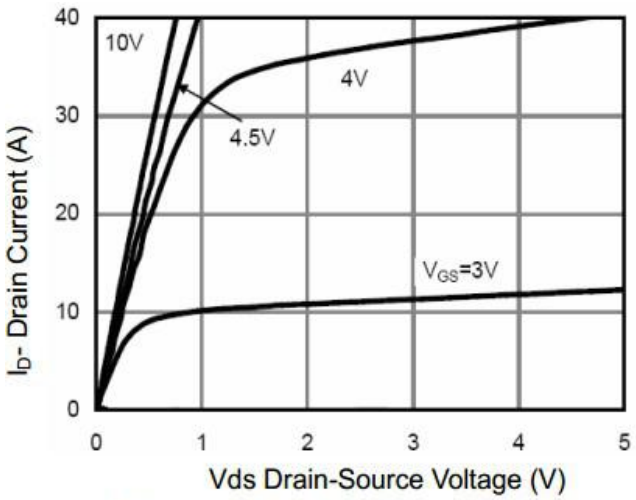


Figure 1 Output Characteristics

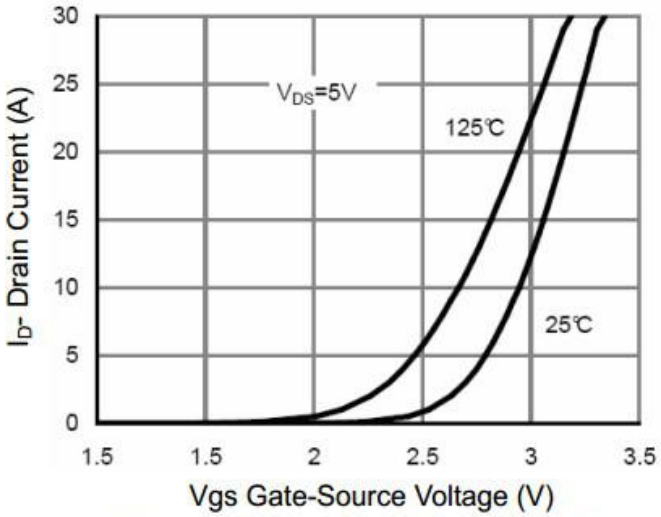


Figure 2 Transfer Characteristics

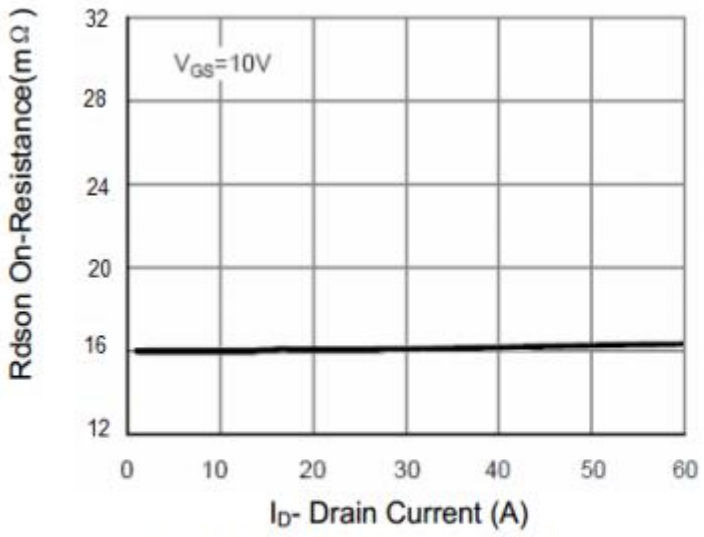


Figure 3 Rdson- Drain Current

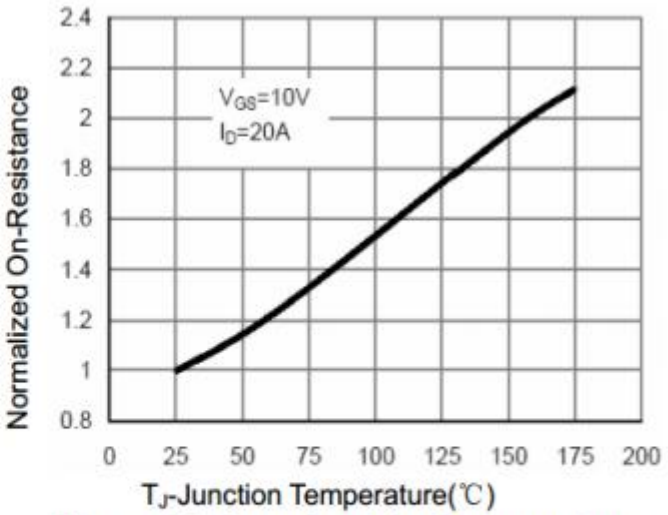


Figure 4 Rdson-Junction Temperature

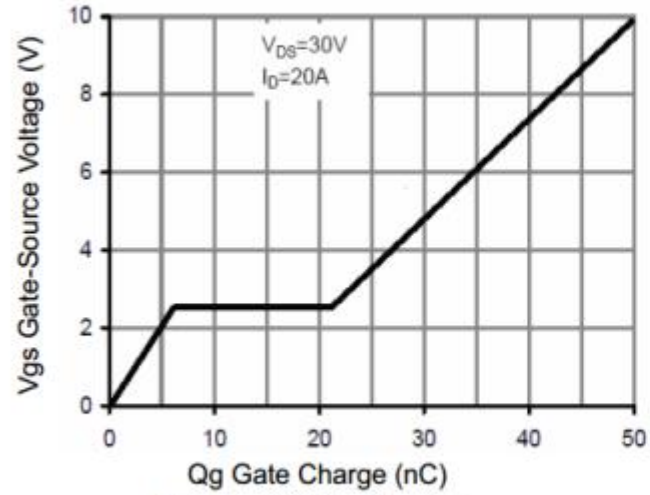


Figure 5 Gate Charge

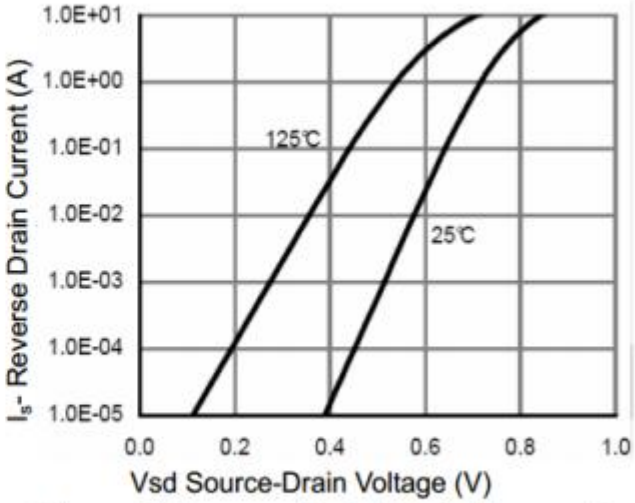


Figure 6 Source- Drain Diode Forward

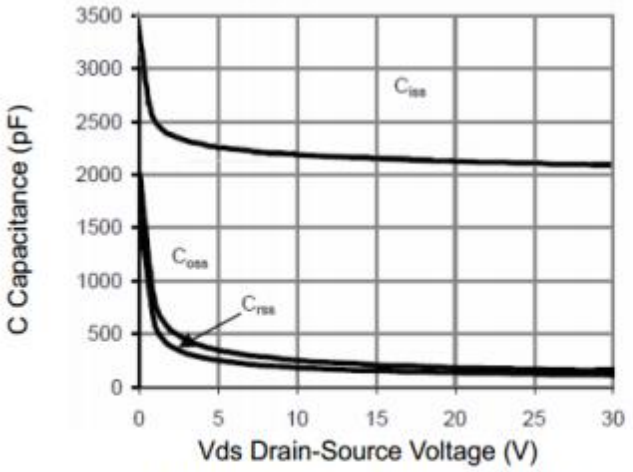


Figure 7 Capacitance vs Vds

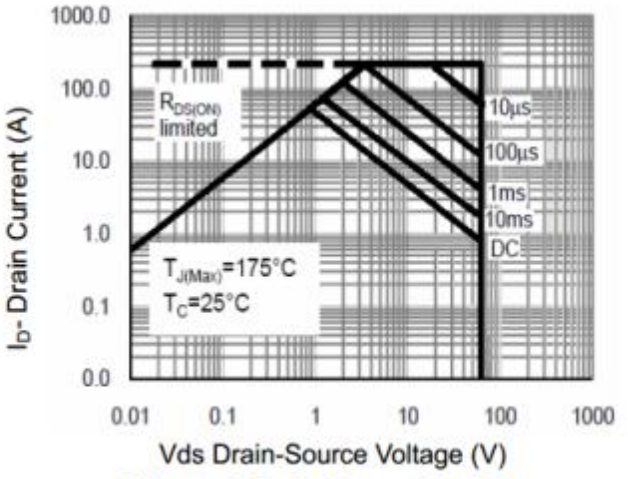


Figure 8 Safe Operation Area

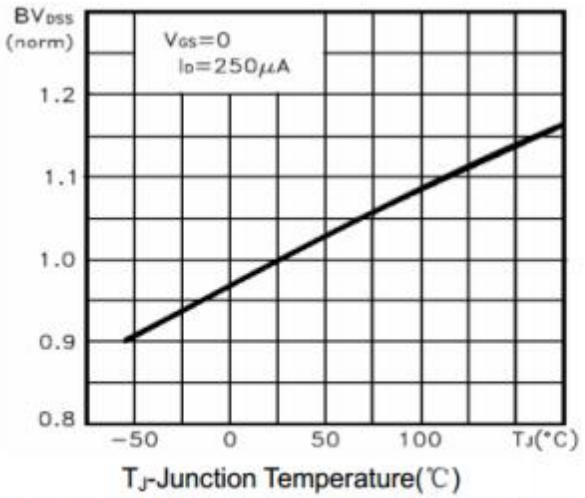


Figure 9 BV_{DSS} vs Junction Temperature

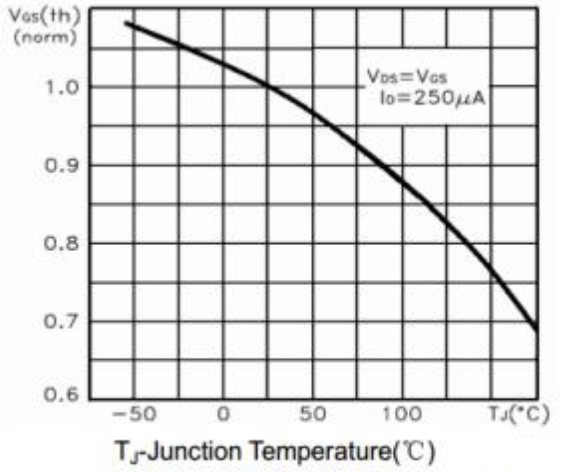


Figure 10 $V_{GS(th)}$ vs Junction Temperature

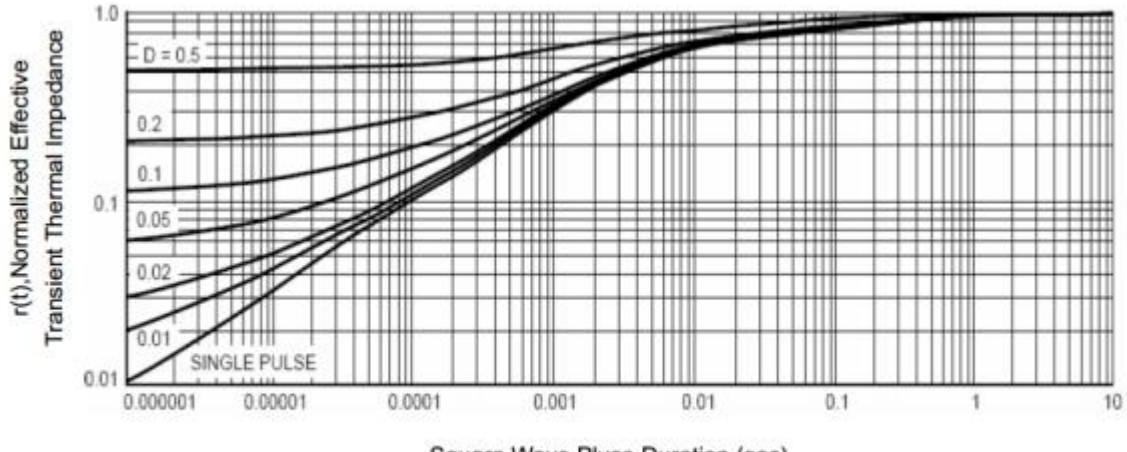
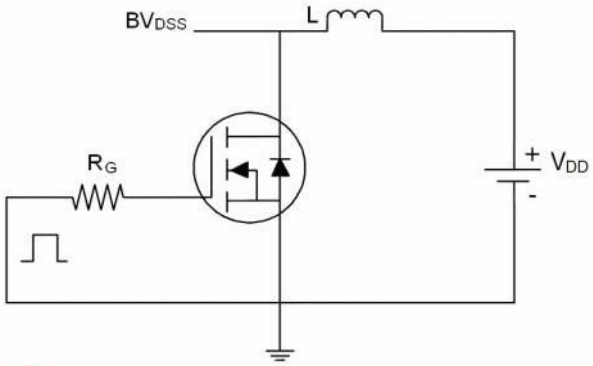


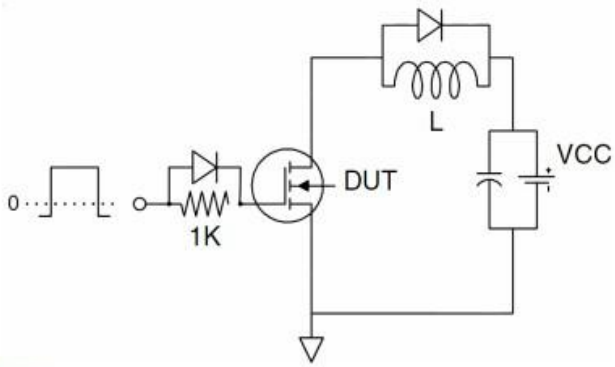
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

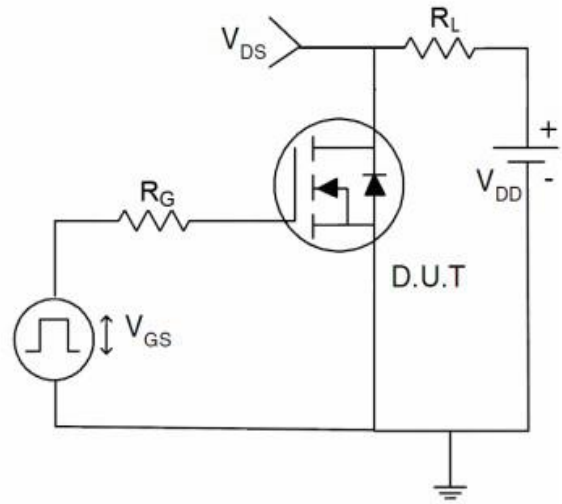
1) E_{AS} test Circuit



2) Gate charge test Circuit

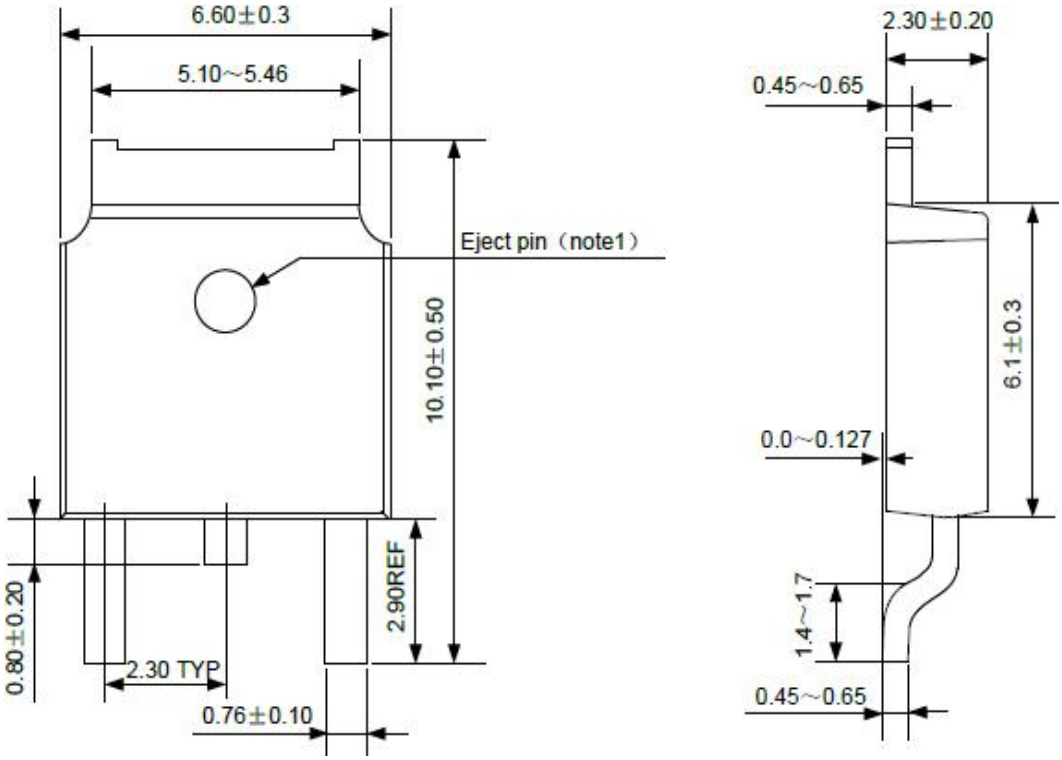


3) Switch Time Test Circuit



Package Outline: TO-252

Unit:mm



Note: The location is divided into top pinhole with no top pinhole two conditions

TO-252 FOOTPRINT：